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Jeong-Hwan Yang	:	Group Art Unit 2812
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Title: SEMICONDUCTOR DEVICE WITH DIFFERENT LATTICE PROPERTIES

SUBMISSION OF ENGISH LANGUAGE TRANSLATION OF FOREIGN-LANGUAGE PRIORITY APPLICATION

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Signed this 21 day of October, 2005.

Young Woo Park
(signature of translator)

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Date of Application : March 17, 2003

Applicant : Samsung Electronics Co., Ltd.

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COMMISSIONER

PATENT APPLICATION

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Title of the Invention:

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Dated this: April 10, 2003

To the COMMISSIONER

[ABSTRACT]

[ABSTRACT]

A semiconductor device capable of reducing a current loss through a channel and improving electron mobility and a method of manufacturing the semiconductor device are disclosed. A first semiconductor layer and a second semiconductor layer having a lattice property different from that of the first semiconductor layer are sequentially formed on a semiconductor substrate. The first semiconductor layer and the second semiconductor layer are subsequently etched to form a first semiconductor pattern. A third semiconductor layer having a lattice property substantially identical to that of the first semiconductor layer is formed on the first semiconductor pattern. The third semiconductor layer is then etched to form a second semiconductor pattern. Thereafter, a gate is formed on the second semiconductor pattern. A contact surface between the second semiconductor pattern and the gate pattern is increased to reduce a current loss, and the lattice property is changed to improve electron mobility of the semiconductor layers.

[REPRESENTATIVE FIGURE]

FIG. 7

[SPECIFICATION]

[TITLE OF THE INVENTION]

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[BRIEF DESCRIPTION OF THE DRAWINGS]

FIG. 1 is a graph illustrating an increase of electron mobility using strained silicon in a conventional semiconductor device.

FIGS. 2 to 7 are process views illustrating a method of manufacturing a semiconductor device according to one embodiment of the invention.

FIG. 8 is a perspective view illustrating a semiconductor device according to one embodiment of the invention.

FIG. 9 is a cross-sectional view illustrating a contact surface between the channel and the gate shown in FIG. 8.

FIG. 10 is a schematic view illustrating a current flow through the channel shown in FIG. 8.

FIG. 11 is a schematic perspective view illustrating a three-dimensional channel emerged from a two-dimensional channel using strained silicon.

<explanation of reference numerals of main elements in the drawings>

100 : a semiconductor substrate	110 : a first semiconductor layer
120 : a second semiconductor layer	130 : a third semiconductor layer
200 : a semiconductor pattern	300 : a second semiconductor pattern
400 : a gate	510 : a first structure
511, 512, 513 : gate contact surfaces	520 : a second structure
520 : a second structure	601 : a general silicon lattice
602 : a strained silicon lattice	710 : a first silicon pattern
720 : a silicon-germanium pattern	730 : a second silicon pattern

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[THE FIELD TO WHICH THE INVENTION PERTAINS AND THE PRIOR ART]

The present invention relates to a semiconductor device and a method of manufacturing the same, and more particularly to a semiconductor device capable of reducing a current loss by increasing the contact surface between a channel and a gate

pattern and capable of improving the electron mobility by changing a lattice property of the channel of a semiconductor layer, and a method of manufacturing the same.

Semiconductor technology has been advanced to develop semiconductor industry. A critical technique for manufacturing the semiconductor is a scaling down and integration technique of a semiconductor transistor. The scaling down and integration technique of a semiconductor transistor is achieved by downsizing the structures forming the semiconductor device. As the semiconductor transistor becomes minute and downsized, more electronic devices are integrated in a unit chip, and the time for electrons to pass the electronic devices is decreased so as to reduce the process time of the electronic devices. Moreover, quantities of the electrons flowing through the semiconductor device are decreased, thereby reducing electric power consumption of the semiconductor transistor.

A high integration, a high speed and a low electric power consumption of the semiconductor device have improved the semiconductor performance. A minimum width of the semiconductor transistor has been changed from 10㎛ in 1971, to 0.25㎛ in 1997, and to 90㎚ in 2003. For the recent 30 years, the semiconductor device has been downsized by about 50 times, and the semiconductor device has been integrated by about 10,000 times. A chip speed of the semiconductor device has been improved by about 1,000 times. Currently, the transistor having a width of about 90㎚ is being researched, and the transistor having a width of about 65㎚ is expected.

During the semiconductor manufacturing process having a transistor with a width of about 0.13㎛, a gate having a width of about 70㎚ has been formed on a wafer having a diameter of about 200㎜. As a wafer having the transistor with the width of about 90㎚ has been produced, a gate having a width of about 50㎚ has been formed on a wafer having a diameter of about 300㎜. During the semiconductor manufacturing process having a transistor with a width of about 65㎚, a gate having a width of about 35㎚ is expected to be formed on a wafer having a diameter above about 300㎜.

The process for manufacturing the semiconductor having the transistor with the width of about 90㎚ has advantages compared to the process for manufacturing the semiconductor having the transistor with the width of about 0.13㎛. Based on fabrication

techniques of a gate oxide layer having a thickness of about 1.2㎚, a gate having a width of about 50㎚ and strained silicon, a high speed and low electric power consumption transistor is produced, and manufacturing cost of the semiconductor device is reduced using the wafer having the diameter of about 300㎜. The semiconductor technology seems to advance henceforth. Despite the rapid progress of the semiconductor technology, a transistor in a chip is still a metal oxide silicon field effect transistor (MOSFET). A principle of the semiconductor operation, which is described by an equation of motion of drift diffusion of an electron as a particle, has been maintained, while the semiconductor device has been downsized by more than 50 times. In other words, the MOSFET fabrication technique is a basis for the downsizing technique.

The minimum width of the transistor is estimated to be about 0.1㎛ according to the MOSFET fabrication technique. However, some problems exist concerning fabrication techniques of the MOSFET having a width below about 0.1㎛. Moreover, when the minimum width of the transistor is about 10 ㎚, in view of physics, a quantum mechanical movement of the electron dominates, and the transistor based on the classical theory considering the electron as an individual charge may not operate.

To solve the problem, two solutions are suggested in view of time based on a technique for fabricating a nano-scale device.

The first solution is to develop the current MOSFET fabrication technique to reduce a short channel effect or side effects due to a quantum effect in an aspect of medium-term, and the second solution is to develop a nano-scale device involving a quantum mechanical operation theory emerged from the classical MOSFET operation theory in an aspect of long-term.

Manufacturing technique of a CMOS transistor having a width below about 0.1㎛ has some obstacles due to a limited space charge layer, a tunneling effect and non uniform doping. Techniques having difficulty, for example, are a lithography, a gate oxide layer, shallow source/drain extension and a technique for forming a halo pocket/retrograde well.

Consequently, a high permittivity gate oxide layer substitutable for SiO2, a technique for improving gate delay, a technique for reducing scattering on a surface

between the gate oxide layer and a channel so as to increase electron mobility and maintain high driving current have been researched without showing no prominent results.

Strained silicon may be used in the semiconductor device during the manufacturing process of the semiconductor having the transistor with the width of about 90㎚.

FIG. 1 is a graph illustrating an increase of electron mobility using the strained silicon in the conventional semiconductor device. The graph is a result of the strained silicon semiconductor test conducted by Intel Corporation. In FIG. 1, a vertical axis represents an effective mobility, and a longitudinal axis represents a vertical effective field.

Referring to FIG. 1, the cases for using a general silicon semiconductor 10, using the silicon strained with silicon-germanium having about 15% germanium atom concentration 15, and using the silicon strained with silicon-germanium having about 20% germanium atom concentration 16 are depicted.

Generally, a semiconductor device is used in a range between about 500 and about 600K V/Cm. A typical silicon semiconductor 10 represents about 270 ㎠/V°s of electron mobility. When the silicon is strained with the 15% silicon-germanium 15, the electron mobility is about 450 ㎠/V°s. When the silicon is strained with the 20% silicon-germanium 16, the electron mobility is about 480 ㎠/V°s.

As shown in FIG. 1, when an active silicon layer is strained with a silicon-germanium epitaxial layer having about 17% germanium atom concentration, the electron mobility increases by over about 70%. The semiconductor device in FIG. 1 is tested in a two-dimensional way. The matching technique of the strained silicon with the transistor in a three-dimensional way has not been developed.

Until now, the two-dimensional method of improving the transistor speed using the strained silicon in the semiconductor device has been known. In order to improve the transistor integrity and speed, it is required to reduce semiconductor device scale or develop a three-dimensional method. Reducing the semiconductor device scale has some limitations since the shape description technique for an integrated circuit has not been secured in a scale less than about 100㎚. Thus, it is preferable to adopt a three-

dimensional device. When the channel width is below about 90㎚, however, a short channel effect and a current leakage through the gate oxide layer may occur. The short channel effect indicates a reduction of an effective channel length due to a diffusion of n-type or p-type impurity atoms in the channel by a heat treatment at a high temperature. When the effective channel length is reduced, a short circuit occurs between the source and the drain in the device having the gate with a minute length.

Poly gates are formed on three faces of the channel transistor in the CMOS structure. The transistor having this structure is called as a Tri-Gate device. The Tri-Gate device may decrease the short channel effect that frequently occurs in a single gate. As is described above, the Tri-Gate device using the strained silicon is very powerful for embodying the transistor having the width below about 90 ㎚. However, the Tri-Gate device has not been yet embodied for the short channel effect and the current leakage through the gate oxide layer.

[TECHNICAL OBJECT OF THE INVENTION]

The present invention is invented to overcome the above-described problems. The first object of the present invention is to provide a semiconductor device and a method of manufacturing the same capable of increasing a contact surface between a gate and a channel to reduce a current loss, and changing a lattice property of a semiconductor layer in the channel to improve electron mobility.

The second object of the present invention is to provide a semiconductor device and a method of manufacturing the same capable of increasing a surface contacting a gate, improving a lattice property of a semiconductor layer and current flow through a channel, and reducing electric power consumption of the semiconductor device.

[CONTRUCTION OF THE INVENTION]

According to embodiments of the present invention, a method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region includes: forming recess gate holes in the substrate within the cell region; forming a gate oxide layer in the recessed gate holes and in the peripheral region; forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and simultaneously patterning the gate layer and the gate

oxide layer to form recessed cell gate structures in the cell region and planar cell gate structures in the peripheral region.

According to further embodiments of the present invention, a method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region includes: forming recess gate holes in the substrate within the cell region and the periphery region; forming a gate oxide layer in the recessed gate holes; forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and simultaneously patterning the gate layer and the gate oxide layer to form recessed cell gate structures in the cell region and in the periphery region.

According to still further embodiments of the present invention, a method for forming a memory device in a semiconductor substrate having a cell region and a periphery circuit region that is separate from the cell region includes: forming a disposable layer disposed on the semiconductor substrate; forming a first set of gate patterns in the disposable layer over the cell region; forming a gate forming hole in the disposable layer over the periphery region; forming recess gate holes in the substrate within the cell region through the first set of gate patterns; forming a gate oxide layer in the recessed gate holes and in the gate forming hole; forming a gate layer on the gate oxide layer in both the cell region and the periphery region; and removing the disposable layer to form recessed cell gate structures in the cell region and cell gate structures in the peripheral region.

According to still further embodiments of the present invention, a memory device includes: a substrate divided into a memory cell region and a peripheral circuit region; a plurality of memory cells having recessed gates formed in the memory cell region; and at least one transistor in the peripheral circuit region. The transistor includes a channel region formed between a source region and a drain region, a gate structure disposed over the channel region, and a resistance-reducing layer formed over the source and drain regions.

According to still further embodiments of the present invention, a method for forming a memory device on a substrate having a memory cell region and a peripheral region includes: growing isolation structures to define a plurality of memory cells in the memory cell region, and to define a plurality of transistors in the peripheral region;

forming a pad oxide layer on the substrate in both the memory cell region and the peripheral region; forming an etch stopping layer on the pad oxide layer; forming a protective oxide layer on the pad oxide layer; depositing a photoresist layer over the protective oxide layer; forming a recess mask in the photoresist layer in the memory cell region; etching the substrate in the memory cell region through the recess mask to form a plurality of recessed gate holes; removing the protective oxide layer, the pad oxide layer, and the etch stopping layer; forming a gate oxide layer in both the memory cell region and the peripheral region, the gate oxide layer penetrating the plurality of recessed gate holes in the cell region; forming a gate layer on the gate oxide layer, including within the plurality of recessed gate holes; and simultaneously forming recessed gates for the plurality of memory cells and planar gates for the plurality of transistors in the peripheral region.

According to still further embodiments of the present invention, a memory device includes: a substrate divided into a cell region and a peripheral region; a plurality of memory cells formed in the cell region, the plurality of memory cells each having a recessed gate structure; and a plurality of transistors in the peripheral region, the plurality of transistors each having a recessed gate structure.

In the following detailed descriptions, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

Embodiments of the invention provide an increase in effective channel length, a decrease in channel dosing, and improved qualities in junction leakage and data retention time in a memory circuit that includes at least two types of transistors on a single substrate: transistors having a recessed gate, and transistors having a planer gate electrode.

EMBODIMENT 1

FIGS. 2 to 7 are views illustrating a method of manufacturing a semiconductor device according to one embodiment of the invention.

Referring to FIGS. 2 and 3, a first semiconductor layer 110 is formed on a

semiconductor substrate 100, and a second semiconductor layer 120 is formed on the first semiconductor layer 110. The second semiconductor layer 120 has a lattice property different from that of the first semiconductor layer 110.

Referring to FIG. 4, the first semiconductor layer 110 and the second semiconductor layer 120 are etched to form a first semiconductor pattern 200 on the semiconductor substrate 100. The first semiconductor pattern 200 includes a first semiconductor layer pattern and a second semiconductor layer pattern.

Referring to FIG. 5, a third semiconductor layer 130 having a lattice property substantially identical to that of the first semiconductor layer 110 is formed on the semiconductor pattern 200. The third semiconductor layer 130 is formed on the semiconductor substrate 100 covering the first semiconductor pattern 200.

Referring to FIG. 6, the third semiconductor layer 130 is etched to form a second semiconductor pattern 300 covering a top surface and sidewalls of the first semiconductor pattern 200.

Referring to FIG. 7, a gate layer (not shown) is formed on the semiconductor substrate 100 having the second semiconductor pattern 300, and the gate layer is etched to form a gate 400 substantially perpendicular to the second semiconductor pattern 300.

The semiconductor substrate 100 is an insulation substrate including an oxide layer, and the first semiconductor layer 110 includes silicon. The first semiconductor layer 110 preferably has a thickness of about 10 to 30㎚.

The second semiconductor layer 120 induces a crystal structure change of the first semiconductor layer 110. In other words, the second semiconductor layer 120 has the lattice property different from that of the first semiconductor layer 110. The second semiconductor layer 120 modifies the crystal structure of the first semiconductor layer 110 since the second semiconductor layer 120 and the first semiconductor layer 110 including different materials that have different crystal structures are formed. Accordingly, the second semiconductor layer 120 may change the crystal structure of the first semiconductor layer 110. When the first semiconductor layer 110 includes silicon, the second semiconductor layer 120 includes silicon germanium or silicon carbide in order to modify the crystal structure of the silicon. The layer of silicon germanium or silicon carbide may apply a tensile force to the lower silicon.

When the first semiconductor layer 110 including silicon is formed, the second semiconductor layer 120 including silicon germanium is preferably formed. The second semiconductor layer 120 including silicon germanium serves as a strain inducing layer, and the first semiconductor layer 110 including silicon forms a strained layer. The first semiconductor layer 110 is referred to as a strained silicon layer hereinafter.

The second semiconductor layer 120 may be formed on the first semiconductor layer 110 in alternative ways. The second semiconductor layer 120 may be formed either by a deposition process or by an epitaxial growth process. The second semiconductor layer 120 is preferably formed on the first semiconductor layer 110 by the epitaxial growth process. Here, the second semiconductor layer 120 has a thickness of about 10 to about 90nm.

After the first and second semiconductor layers 110 and 120 are sequentially formed on the semiconductor substrate 100, the first and second semiconductor layers 110 and 120 are etched through a photolithography process so as to form the first semiconductor pattern 200. The first semiconductor pattern 200 is formed on the semiconductor substrate 100 in a first direction that is a longitudinal direction of the semiconductor substrate 100.

After the first semiconductor pattern 200 is formed, the third semiconductor layer 130 is formed on the first semiconductor pattern 200. The third semiconductor layer 130 is etched through the photolithography process so as to form a third semiconductor layer pattern 131 on the top surface and on the sidewalls of the first semiconductor pattern 200 completing the second semiconductor pattern 300. The third semiconductor layer pattern 131 covers the second semiconductor pattern 300. The third semiconductor layer 130 has the lattice property substantially identical to that of the first semiconductor layer 110. For example, when the first semiconductor layer 110 including silicon is formed, the third semiconductor layer 130 including silicon that has the lattice property substantially identical to that of the first semiconductor layer 110 is formed. In other words, the third semiconductor layer 130 including a material having a crystal structure substantially identical to that of the first semiconductor layer 110 is formed. However, the material forming the third semiconductor layer 130 may not substantially identical to the material forming the first semiconductor layer 110.

The method of forming the second semiconductor pattern 300 varies accordance with the method of forming the third semiconductor layer 130. When the third semiconductor layer 130 is deposited on the second semiconductor pattern 300 of the semiconductor substrate 100, the second semiconductor pattern 300 is formed through the photolithography process.

The third semiconductor layer 130 may be formed from the first semiconductor pattern 200 including silicon through the epitaxial growth process. A pre-baking or pre-cleaning process is performed before the epitaxial growth process of the first semiconductor pattern 200 is performed. The pre-baking or pre-cleaning process is performed so as to prevent growing of a natural oxide layer when the silicon is exposed. In the pre-baking or pre-cleaning process, the semiconductor substrate 100 is heated for about 1 minute at a temperature of about 900℃. Then, the epitaxial growth process is performed. In the epitaxial growth process, the semiconductor substrate 100 is heated for about less than two minutes at a temperature of about 900℃. The third semiconductor layer 130 formed by the epitaxial growth process preferably has a thickness of about 10 to about 100㎚. The epitaxial growth process is performed in a simpler way than the photolithography process. When the first semiconductor pattern 200 including silicon epitaxially grows, silicon family material grows on an outer face of the first semiconductor pattern 200. The silicon family material formed on the first semiconductor pattern 200 has a lattice property substantially identical to that of silicon.

The semiconductor substrate 100 is an insulation substrate including an oxide layer, and the first semiconductor layer 110 is a silicon layer. The second semiconductor layer 120 is preferably a silicon-germanium layer grown from the first semiconductor layer 110, and the third semiconductor layer 130 is preferably a silicon layer epitaxially grown form the first semiconductor pattern 200. The second semiconductor layer 120 has vertically grown from the surface of the first semiconductor layer 110. A germanium concentration in the silicon germanium gradually increases from the first semiconductor layer 110.

After the second semiconductor pattern 300 is formed, a gate oxide layer is formed on the second semiconductor pattern 300. Materials constituting the gate are sequentially formed on the gate oxide layer, and then planarized and etched through a wet

etching or dry etching process so as to form the gate 400. The second semiconductor pattern 300 serves as a channel contacting the gate 400. A layer forming a spacer is then deposited on the gate 400 and etched to form the spacer.

A metal layer is deposited on the gate 400, and heat treatment is carried out to form a metal silicide layer on the gate 400. Examples of the metal deposited on the gate 400 include cobalt (Co), nickel (Ni), lead (Pb), etc. As a design rule of the semiconductor device has been reduced, it has been necessary to form the metal silicide layer in the semiconductor device.

One end of the second semiconductor pattern 300 makes contact with a source region of the semiconductor substrate 100, and the other end of the second semiconductor pattern 300 makes contact with a drain region of the semiconductor substrate 100. The second semiconductor pattern 300 serves as a channel between the source that is a cathode and the drain that is an anode. The channel including electric conductive silicon is formed so as to serve as a current path. The gate oxide layer is formed on the contact surface between the gate 400 and the outer face of the second semiconductor pattern 300 to connect the gate 400 with the channel.

Generally, it is required to use a three-dimensional semiconductor device or to reduce a scale of the semiconductor device in order to increase transistor integrity and speed. In the three-dimensional semiconductor device, when a channel width is below about 90㎚, current leakage occurs through the gate oxide layer.

The second semiconductor pattern 300, i.e., the channel, has a three-dimensional structure, and the gate 400 covers the second semiconductor pattern 300. Thus, a contact surface between the channel and the gate may be increased. In other words, a tri-gate structure is formed along three sides of the channel. Problems related with a silicon thickness and current leakage are alleviated in the tri-gate structure than in a single gate structure. Here, the second semiconductor pattern 300, the gate oxide layer, the gate 400, the spacer, the source region, the drain region, and the metal silicide layer are structures for operating the metal oxide silicon field effect transistor (MOSFET).

In the MOSFET, a gate is formed on a surface of p-type silicon substrate. A source and a drain are formed near the surface of the substrate. A channel, which serves as a current path between the source and the drain, is formed. When negative voltages are

applied to the gate, holes in the substrate are attracted in one direction to gather in the channel to increase the current between the source and the drain. On the other hand, when positive voltages are applied to the gate, the holes are repulsed from the gate to decrease the current between the source and the drain. When more positive voltages are applied to the gate, however, electrons in the semiconductor gather in the channel to increase the current between the source and the drain. The MOSFET amplifies the current flowing through the channel depending on the gate voltage condition.

The depth of the source and the drain is reduced as the semiconductor becomes minute. Accordingly, resistance in the source region and the drain region increases in a minute semiconductor device to impair the MOSFET device. On the other hand, the semiconductor device according to the present invention includes the second semiconductor pattern 300 and the channel vertically formed in the three-dimensional structure to connect the source region and the drain region. Thus, impair of the MOSFET due to the increased resistance may be prevented. The method of manufacturing the semiconductor device may further include an ion-injection process injecting impurities in each semiconductor layer in order to improve electrical characteristics of the semiconductor device.

EMBODIMENT 2

FIG. 8 is a perspective view illustrating the semiconductor device according to one embodiment of the invention. FIG. 9 is a cross-sectional view illustrating a contact surface between the channel and the gate of FIG. 8. FIG. 10 is a schematic cross-sectional view illustrating a current flow through the channel of FIG. 8. FIG. 11 is a schematic perspective view illustrating a three-dimensional channel emerged from a two-dimensional channel using strained silicon.

As depicted in FIG. 8, the semiconductor device according to the second embodiment of the present invention includes a first structure 510 and a second structure 520 formed on a semiconductor substrate 100. The first structure 510 includes a first semiconductor pattern, and the second structure 520 includes a second semiconductor pattern. The second structure 520 has a lattice property different from that of the first semiconductor, and is positioned penetrating a center of the first structure 510.

A gate oxide layer is formed on an outer face of the first structure 510, and a gate 400 is formed on the first structure 510 substantially perpendicular to the first structure 510. A spacer (not shown) is formed on sidewalls of the gate 400, and a metal silicide layer may be formed on a surface of the first structure 510 and on the gate 400. Examples of the metal deposited on the first structure 510 and the gate 400 include cobalt, nickel, lead, etc. As a design rule of the semiconductor device has been reduced, it has been necessary to form the metal silicide layer in the semiconductor device.

One portion of the first structure 510 makes contact with a source region formed on one portion of the semiconductor substrate 100, and another portion of the first structure 510 makes contact with a drain region formed on another region of the semiconductor substrate 100.

The semiconductor substrate 100 is an insulation substrate including an oxide layer, and the first structure 510 includes silicon. A lower portion of the first structure 510 is formed to have a thickness of about 10 to about 30㎚ from the surface of the semiconductor substrate 100, another portion of the first structure 510 is preferably formed to have a thickness of about 10 to about 100㎚.

The second structure 520 includes the second semiconductor pattern, which induces crystal structure changes of the first structure 510. Accordingly, the second structure 520 has the lattice property different from that of the first structure 510.

The second structure 520 including silicon-germanium or silicon carbide is formed in order to modify the crystal structure of silicon. When the first structure 510 includes silicon, the second structure 520 preferably includes silicon-germanium. The second structure 520 is positioned in a first direction that is a longitudinal direction of the semiconductor substrate 100 penetrating the center of the first structure 510. In other words, the second structure 520 is formed being inserted in the center of the first structure 510 in the longitudinal direction of the semiconductor substrate 100. Here, the second structure 520 is formed from the first structure 510 including silicon through the epitaxial growth process. The second structure 520 is preferably formed to have a thickness of about 10 to about 90㎚.

The gate 400 is formed on the first structure 510 substantially perpendicular to the first structure 510. The gate oxide layer has been formed between the first structure 510

and the gate 400. The first structure 510 serves as a channel contacting the gate 400. The first structure 510, which is the channel, serves as a current path. The first structure 510 is connected to the gate 400 through the gate oxide layer. The first structure 510, the second structure 520, the gate oxide layer, the gate 400, the spacer, the source region, the drain region, and the metal silicide layer are structures for operating the MOSFET. The MOSFET amplifies the current flowing through the channel depending on the gate voltage condition.

When negative voltages are applied to the gate 400, holes in the semiconductor substrate 100 are attracted in one direction to gather in the channel to increase the current between the source and the drain. On the other hand, when positive voltages are applied to the gate 400, the holes are repulsed from the gate 400 to decrease the current between the source and the drain. When more positive voltages are applied to the gate, however, electrons in the semiconductor gather in the channel to increase the current between the source and the drain. In this embodiment, the first structure 510 has a three-dimensional structure, and the gate has three gate contact surfaces 511, 512 and 513. Generally, the depth of the source and the drain is reduced as the semiconductor becomes minute. Accordingly, resistance in the source region and the drain region increases in a minute semiconductor device to impair the MOSFET device. The semiconductor device according to the present invention has increased gate contact surfaces 511, 512 and 513, which contact the gate and the channel, so as to increase transistor integrity and speed. More contact surfaces reduce current leakage through the gate oxide layer.

The second structure 520 modifies the crystal structure of the first structure 510. More particularly, the silicon-germanium included in the second structure 520 induces a tensile force to the silicon included in the first structure 510. This is because lattice constants of the silicon-germanium and the silicon are different. The silicon having modified crystal structure is referred to as strained silicon hereinafter. When the crystal structure of the first structure 510 is modified, resistance of the current passing through the first structure 510 is reduced. As shown in FIG. 10, electron mobility or hole mobility is more improved in the strained silicon lattice 602 than in general silicon lattice 601. This is because the crystal structure of the silicon is modified so as to reduce the resistance in the electrons. Accordingly, a three-dimensional channel is used to improve

the transistor integrity and speed. However, as the channel width decreases, a short channel effect or current leakage through the gate oxide layer occurs. Thus, it is needed to reduce the amount of the gate oxide layer and to increase the current flow. As a result, the three-dimensional channel using the strained silicon is required. The conventional semiconductor channel is a two-dimensional channel having silicon-germanium, which induces silicon strain, between two silicon layers. When the two-dimensional channel using the conventional silicon-germanium is expanded to be a three-dimensional channel, a silicon-germanium pattern 720 is exposed as depicted in FIG. 11. A first silicon pattern 710 and a second silicon pattern 730 are spaced apart and electrically disconnected to each other. A gate oxide layer is formed on the outer face of the channel, and makes contact with the gate. Here, the gate oxide layer should be deposited on the silicon. When the silicon-germanium pattern 720 is exposed outside, an abnormal channel having the gate oxide layer partially formed on the outer surface of the channel is formed. The strain of the first silicon pattern 710 and the second silicon pattern 730 by the silicon-germanium pattern 720 may not proceed uniformly. The silicon-germanium pattern 720 induces strain of the first silicon pattern 710 and the second silicon pattern 730 only on the regions where the silicon-germanium pattern 720 makes contact with the first silicon pattern 710 or the second silicon pattern 730. Strains in the first silicon pattern 710 and the second silicon pattern 730 may not be uniform.

Therefore, the channel according to the present invention has the three-dimensional silicon channel to suppress the short channel effect and improve the current loss through the gate oxide layer. Moreover, the silicon-germanium pattern is formed penetrating the pattern in the silicon channel the longitudinal direction of the semiconductor substrate to improve the electron mobility and reduce electric power consumption.

[THE EFFECT OF THE INVENTION]

According to the present invention, a structure having the lattice property different from that of silicon is formed penetrating the silicon structure. Thus, the contact surface between the channel and the gate is increased, the short channel effect is suppressed, and the current leakage is reduced.

Additionally, the semiconductor device having silicon-germanium is applied to the channel to reduce electron mobility and the current loss in the channel.

Those skilled in the art recognize that the method of forming integrated circuits described herein can be implemented in many different variations. Therefore, although various embodiments are specifically illustrated and described herein, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appending claims without departing from the spirit and intended scope of the invention

[CLAIMS]

[CLAIM 1]

A method of manufacturing a semiconductor device comprising:

sequentially forming a first semiconductor layer and a second semiconductor layer on a semiconductor substrate, the second semiconductor layer having a lattice property different from the first semiconductor layer;

etching the second semiconductor layer and the first semiconductor layer to form a first semiconductor pattern;

forming a third semiconductor layer on the first semiconductor pattern, the third semiconductor layer having a lattice property substantially identical to the lattice property of the first semiconductor layer; and

etching the third semiconductor layer to form a second semiconductor pattern covering the first semiconductor pattern.

[CLAIM 2]

The method of claim 1, wherein the first semiconductor layer comprises silicon, and the second semiconductor layer comprises silicon-germanium.

[CLAIM 3]

The method of claim 2, wherein the second semiconductor layer is formed by an epitaxial growth process.

[CLAIM 4]

The method of claim 2, wherein the third semiconductor layer comprises silicon.

[CLAIM 5]

The method of claim 1, wherein the second semiconductor pattern is formed on a top surface and on sidewalls of the first semiconductor pattern.

[CLAIM 6]

The method of claim 1, further comprising forming a gate on the second

semiconductor pattern, the gate being substantially perpendicular to the first semiconductor pattern.

[CLAIM 7]

The method of claim 6, further comprising forming a gate oxide layer between the gate and the second semiconductor pattern.

[CLAIM 8]

The method of claim 6, further comprising forming a metal silicide layer on a top surface of the gate.

[CLAIM 9]

A method of claim 1, further comprising injecting impurities in the first semiconductor pattern and in the second semiconductor pattern.

[CLAIM 10]

A semiconductor device comprising:

a first structure formed on a semiconductor substrate, the first structure comprising a first semiconductor pattern; and

a second structure formed penetrating the first structure, the second structure having a lattice property different from the lattice property of the first semiconductor pattern.

[CLAIM 11]

The method of claim 10, further comprising:

forming spacer structures on the cell gate structures in the cell region and in the peripheral region; and

wherein etching the layers occurs after forming the spacer structures.

[CLAIM 12]

The semiconductor device of claim 11, further comprising a gate oxide layer formed between the first structure and the gate.

[CLAIM 13]

The semiconductor device of claim 11, further comprising a metal silicide layer formed on a top surface of the gate.

[CLAIM 14]

The semiconductor device of claim 10, wherein a first portion of the first structure makes contact with a source region formed on a first portion of the semiconductor substrate, and a second portion of the first structure makes contact with a drain region formed on a second portion of the semiconductor substrate.

[CLAIM 15]

The semiconductor device of claim 10, the first semiconductor pattern comprises silicon, and the second semiconductor pattern comprises silicon-gernamium.

[CLAIM 16]

The semiconductor device of claim 15, wherein a lower portion of the second structure makes contact with the semiconductor substrate.

[CLAIM 17]

The semiconductor device of claim 16, wherein the second structure further comprises a third semiconductor pattern formed between the second semiconductor pattern and the semiconductor substrate.

[CLAIM 18]

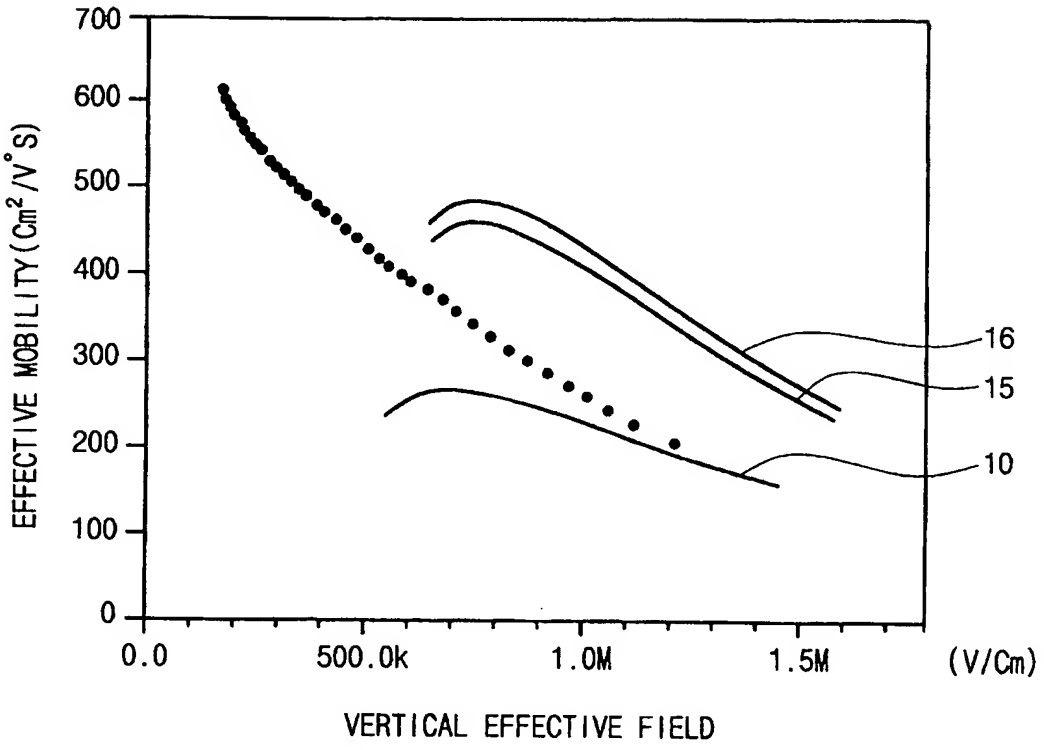
The semiconductor device of claim 17, wherein the third semiconductor pattern has a lattice property substantially identical to the lattice property of the first semiconductor pattern.

[CLAIM 19]

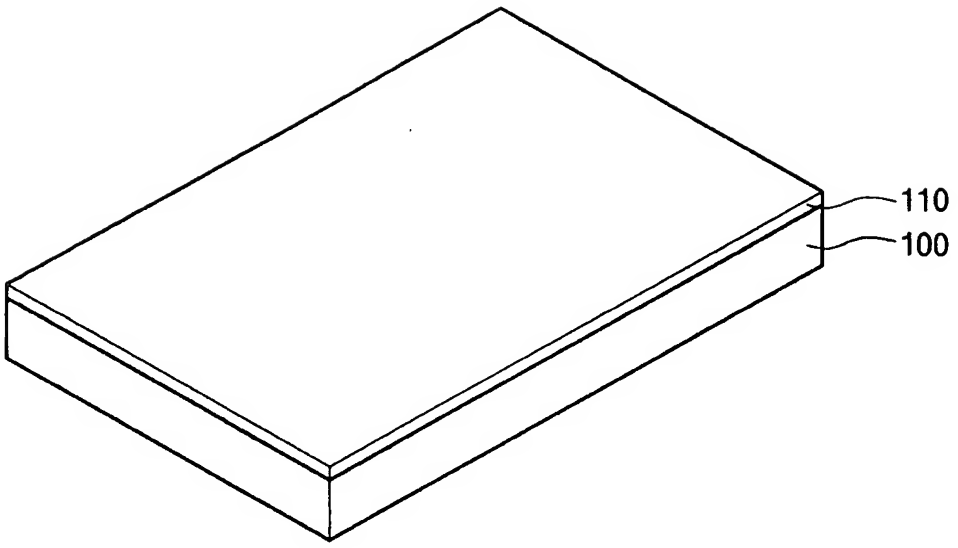
The semiconductor device of claim 18, wherein the third semiconductor pattern comprises silicon.

[DRAWINGS]

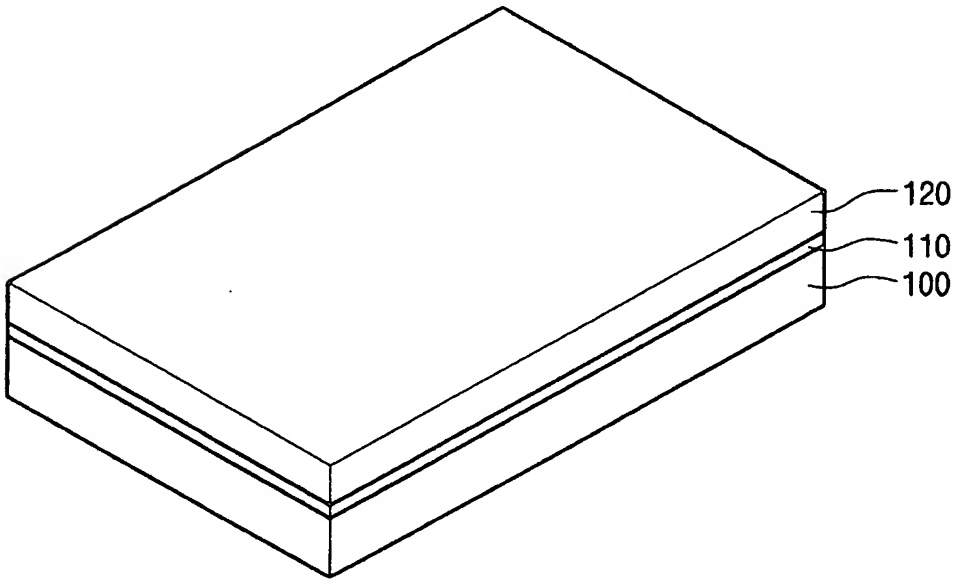
【FIG. 1】



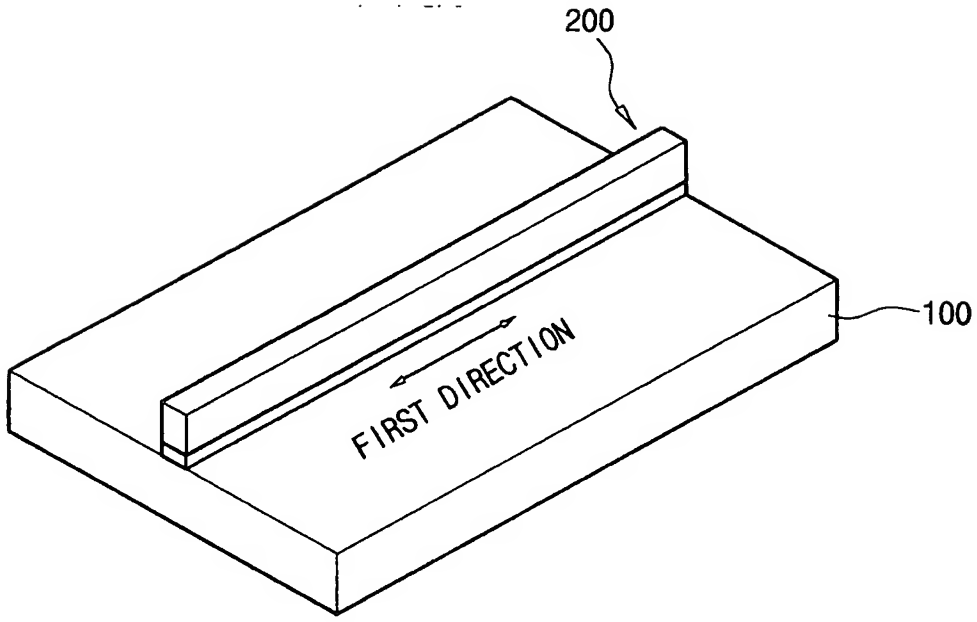
【FIG. 2】



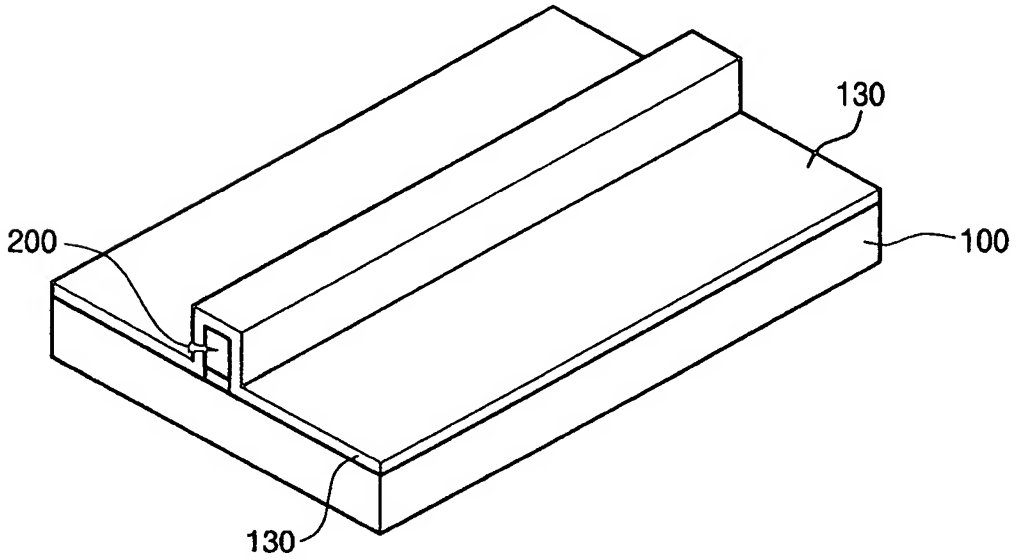
【FIG. 3】



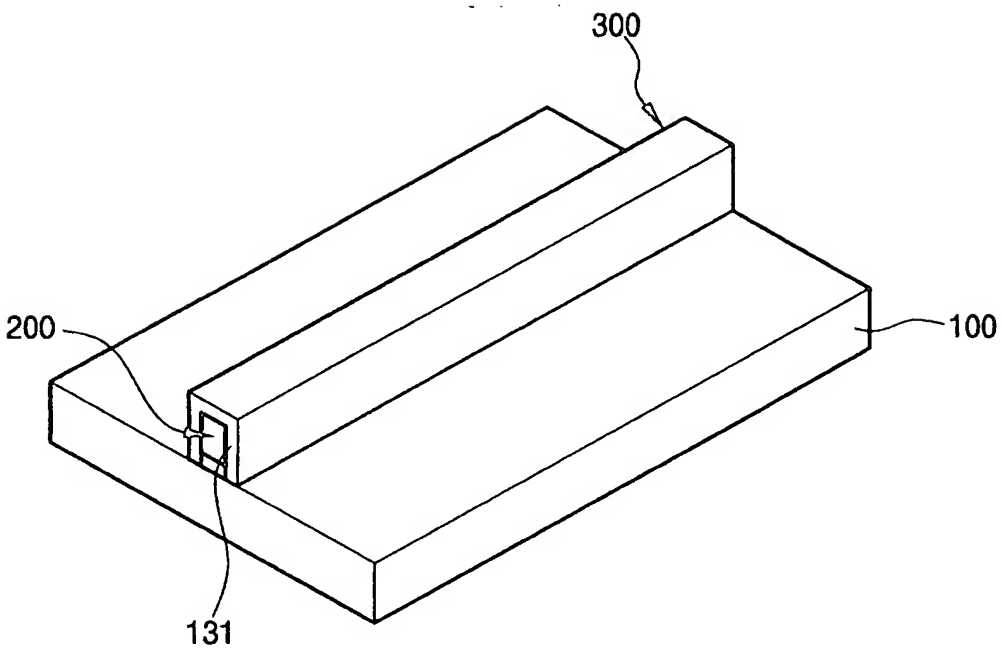
【FIG. 4】



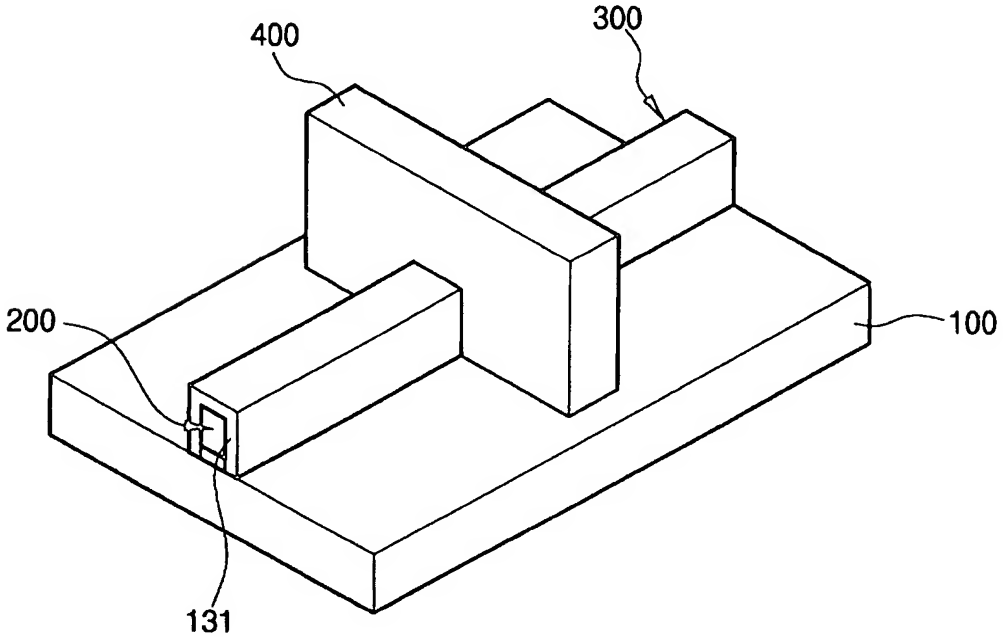
【FIG. 5】



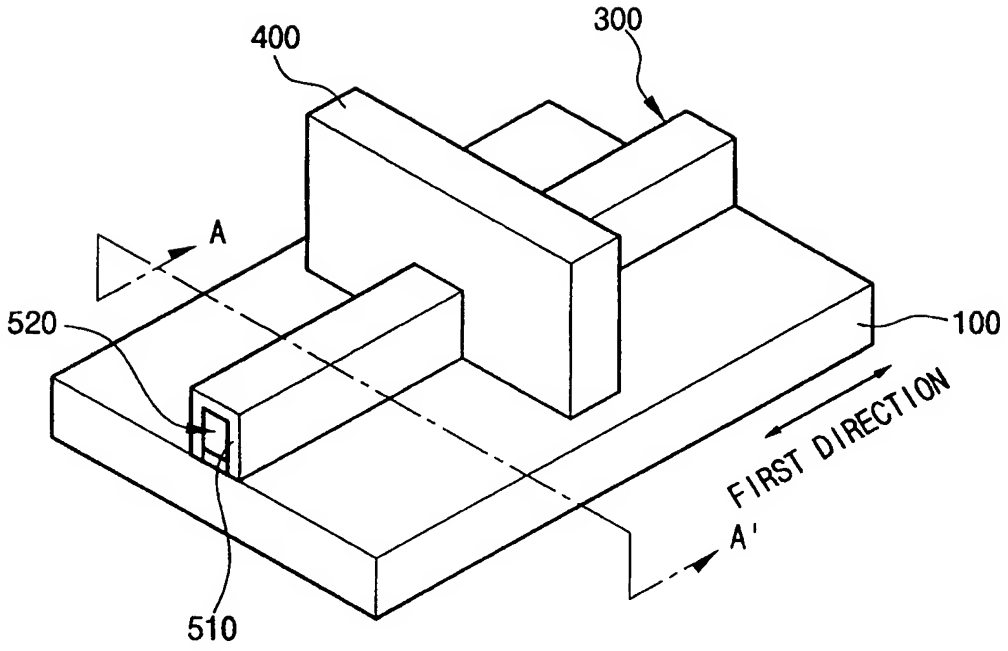
【FIG. 6】



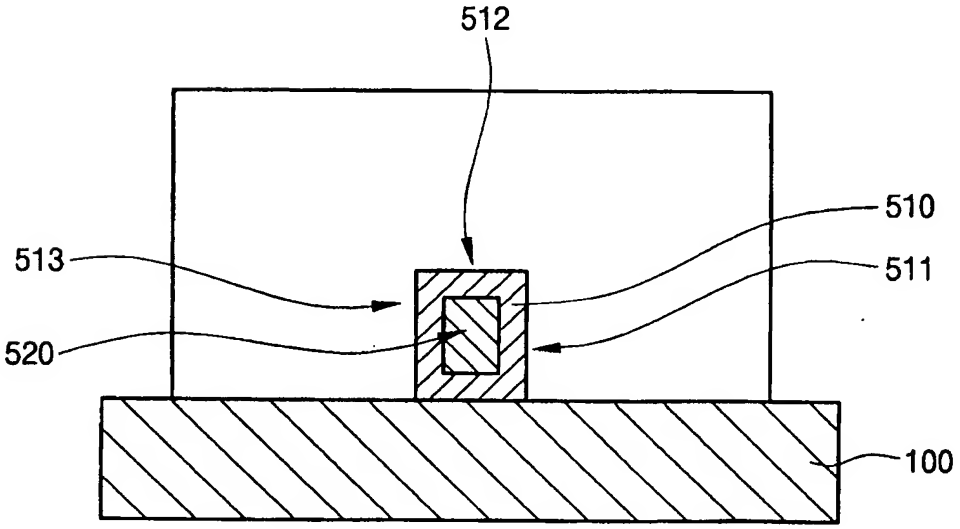
【FIG. 7】



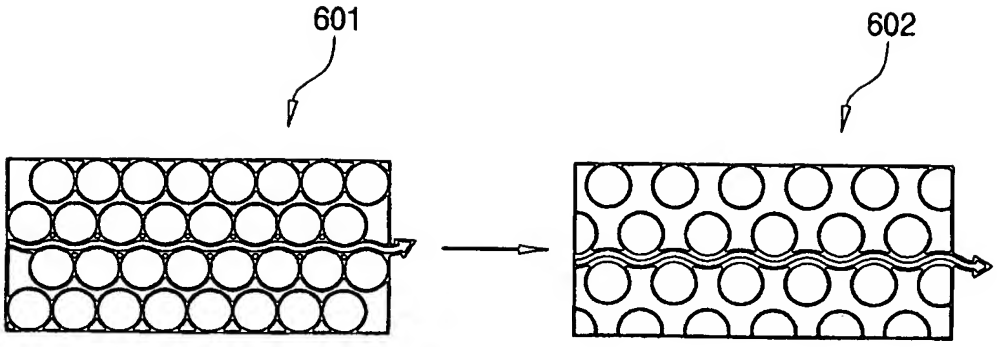
【FIG. 8】



【FIG. 9】



【FIG. 10】



【FIG. 11】